A Comparative Study of Pipelining Techniques for Recursive Filter Implemented in FPGA

Ayesha Firdous, Dr.B.Rajan

Abstract—This paper presents different pipelining approach for higher order recursive digital filter. The performance of the filter is increased by pipelining the filter. Clustered look-ahead, scattered look-ahead pipelining methods and implementation of IIR filter in FPGA are analyzed. Clustered look-ahead pipeline is not always stable. To achieve a stable pipeline filter scattered look-ahead pipelining is used. The second order all pole recursive filter is considered and 3-level pipelined transfer function is obtained using clustered look-ahead and scattered look-ahead pipelining techniques. The filter is implemented in direct form-I structure.

Index Terms— clustered look-ahead pipelining; FPGA; IIR Filter; Pipelining; Power Analysis; Scattered look-ahead pipelining; Xilinx Power Estimator

1 INTRODUCTION

THE different types of filters based on impulse response are FIR and IIR filter. FIR output depends on present and previous input samples.IIR filter output depends on present, past input samples and output samples. It is also called as recursive filter. In IIR filter, specified frequency response can be obtained in lower order compared to FIR filter.FIR filter have storage element to hold the input samples, but the IIR filter need storage element to hold input as well as output samples. In [9], to ensure satisfactory fixed-point operation of the IIR filter, coefficient quantization, internal quantization, overflow and stability are discussed.

2 INFINITE IMPULSE RESPONSE FILTER

The transfer function of Nth-order IIR filter is described by

$$H(z) = \frac{\sum_{i=0}^{N} b_i z^{-i}}{1 + \sum_{i=0}^{N} a_i z^{-i}}$$

Where a_i , b_i are filter coefficients, referred as feedback and feed forward coefficients.

IIR filter can be pipelined to reduce the power consumption and critical path. In this paper pipelining of higher order IIR filter using clustered lo In[5], a universal look-ahead algorithm to find the filter coefficients for pipelining IIR filter is proposed,look-ahead and scattered look-ahead techniques are considered.

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2.1 Clustered Look-Ahead Pipelining

In [7], the basic idea of clustered look-ahead pipelining is to add cancelling poles and zeros to the filter transfer function such that the coefficients of z-1, z-2, …., z-(M-1) in the denominator of the transfer function are zero. For e.g. A 6-stage pipelined realization can be obtained by eliminating z-1, z-2, z-3, z-4, z-5 terms in the denominator of the transfer function. In this technique, if the stability of the filter is changed after pipelining, the number of pipeline stages is increased until a filter is stable.

2.2 Scattered Look-Ahead Pipelining

In this method, if the original filter is stable, the pipelined filter is also stable but it is not in clustered look-ahead pipelining. In scattered look-ahead pipelining, denominator of the transfer function contains $z^{-M}, z^{-2M}, \ldots, z^{-NM}$ terms. In [6], a decomposition technique is proposed to implement the non recursive portion (generated due to the scattered look-ahead process) in a decomposed manner. The upper bound on the round off error in these pipelined filters is shown to improve with an increase in the number of loop pipeline stages.

3 DESIGN EXAMPLE

In this section, the transfer function of 3-level pipelined filter is obtained using clustered look-ahead and scattered look-ahead approach. Consider the 2nd order all pole recursive filter

$$H(z) = \frac{1}{1 - \frac{3}{5}z^{-1} + \frac{1}{4}z^{-2}}$$

3.1 Clustered Look-Ahead Pipelining

A two stage pipelined IIR filter is derived by eliminating z^{-1} denominator of the transfer function. This can be done by multiplying Numerator and denominator by $1+0.6z^{-1}$ .The transfer function of two stage filter is

$$H(z) = \frac{1+\frac{3}{5}z^{-1}}{1-\frac{11}{100}z^{-2}+\frac{3}{20}z^{-3}}$$

3 stage pipelined realization can be derived by eliminating z^{-1} and z^{-2} terms in the denominator of the transfer function. Multiplying numerator and denominator by

$$1+\frac{3}{5}z^{-1}+\frac{11}{100}z^{-2}$$

Transfer function becomes

$$H(z) = \frac{1+0.6z^{-1}+0.11z^{-2}}{1+0.084z^{-3}+0.0275z^{-4}}$$

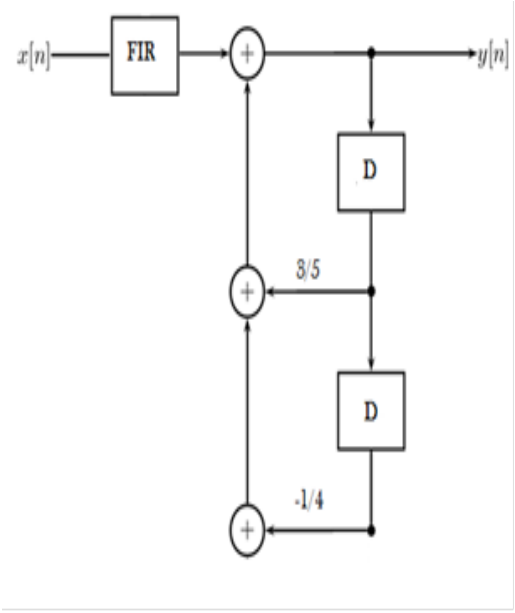

Fig.1. Implementation of non pipelined IIR filter

3.2 Scattered Look-Ahead Pipelining

In 3-stage scattered look-ahead pipelining, denominator of the transfer function contains z-3 and z-6 terms. The transfer function is

$$H(z) = \frac{1+0.6z^{-1}+0.11z^{-2}+0.15z^{-3}+0.0625z^{-4}}{1-0.234z^{-3}+0.0156z^{-6}}$$

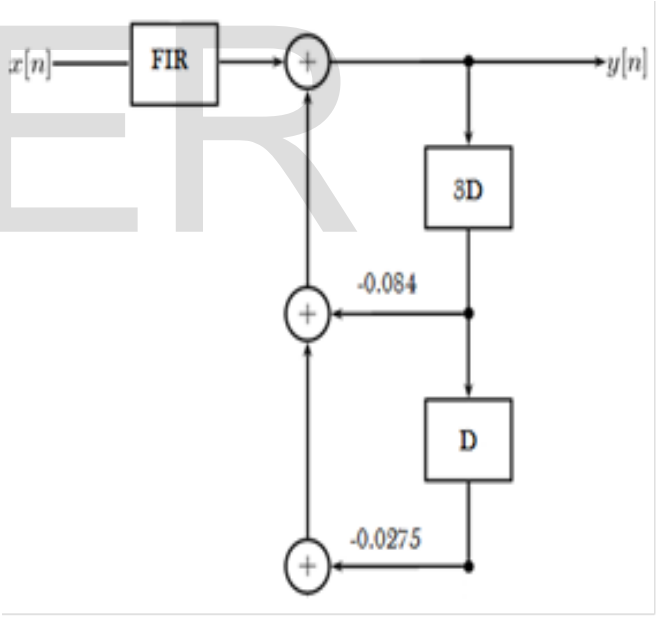

Fig.2. Implementation of clustered look-ahead pipelined IIR filter

4 IIR FILTER STRUCTURE

IIR filter can be implemented in Direct form-I, Direct form-II, cascade form, parallel form, Biquad, etc., In this paper, Direct Form-I structure is considered. It is a straight forward approach; transfer function of the filter can be obtained directly.Fig.1. shows the direct form-I realization of non pipelined filter.Fig.2. and Fig.3. shows the pipelined architecture.

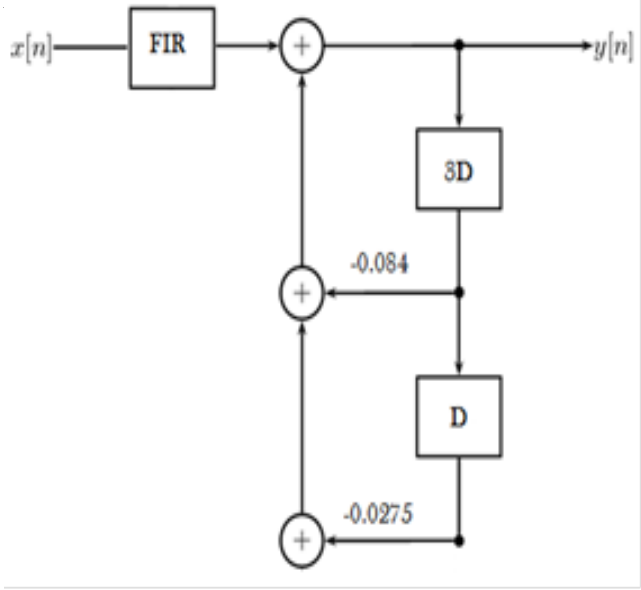

Fig.3. Implementation of scattered look-ahead pipelined IIR filter

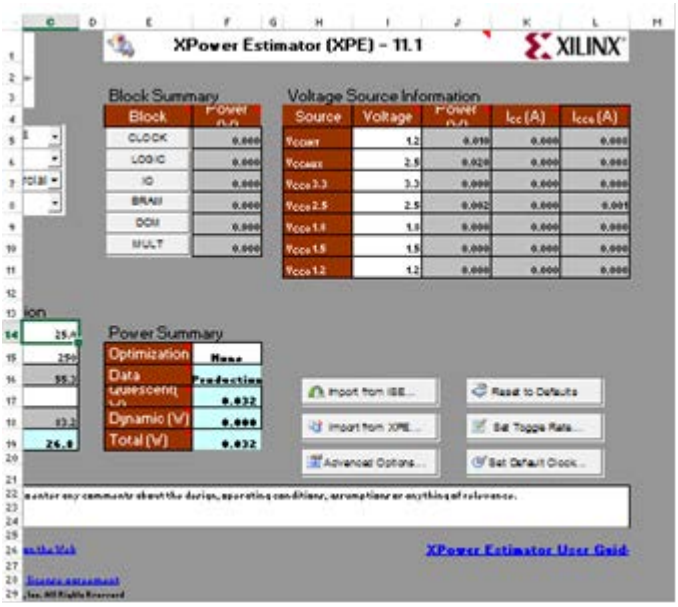

Fig.4. Xilinx Power Estimator

5 IMPLEMENTATION OF IIR FILTER IN FPGA

DSP algorithm can be implemented in FPGA but their performance and density may lag behind that of a special purpose DSP or an ASIC chip. FPGAs, however, afford the benefits of flexibility, reduced NRE costs, rapid prototyping, early market entry and reduced risk [8]. IIR filter can be implemented using system generator for DSP software. System Generator for DSP is a highly productive design environment for the development and prototyping of DSP systems using FPGA[9] In this, filter is designed in simulink environment then HDL code is obtained using system generator and it is synthesized. Finally the bit stream is loaded in FPGA. In [3] a method to implement IIR filter using Xilinx system generator is proposed. IIR filter can be implemented in FPGA without using system generator software.

6 RESULTS

Xilinx Power Estimator tool is used to estimate the power consumption of FPGA. Fig.4. shows the snapshot of XPower Estimator tool. Fig.5 shows output of clustered look-ahead pipelined IIR filter and Fig.6 shows output of scattered look-ahead pipelined IIR filter.

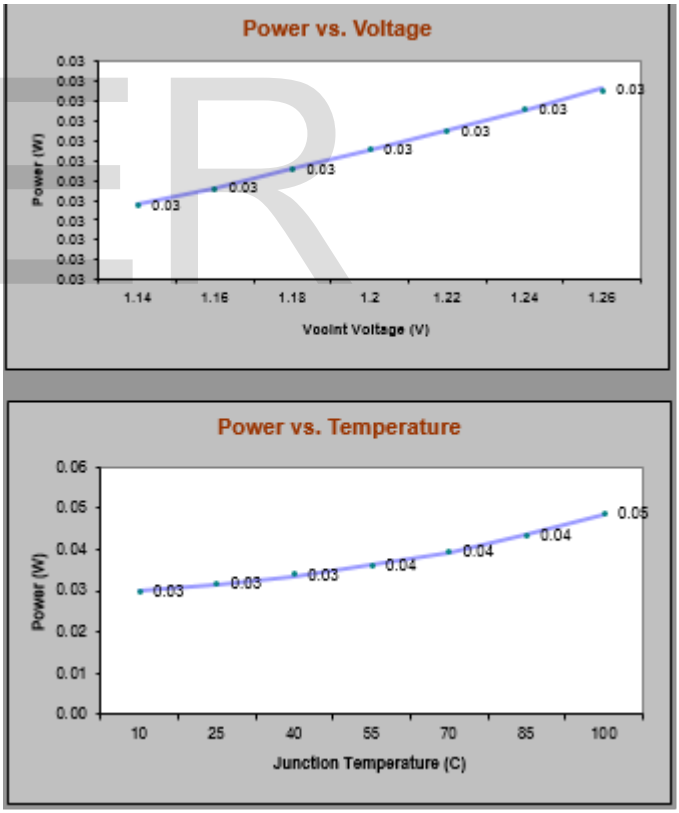

Fig.5 output of clustered look-ahead pipelined IIR filter

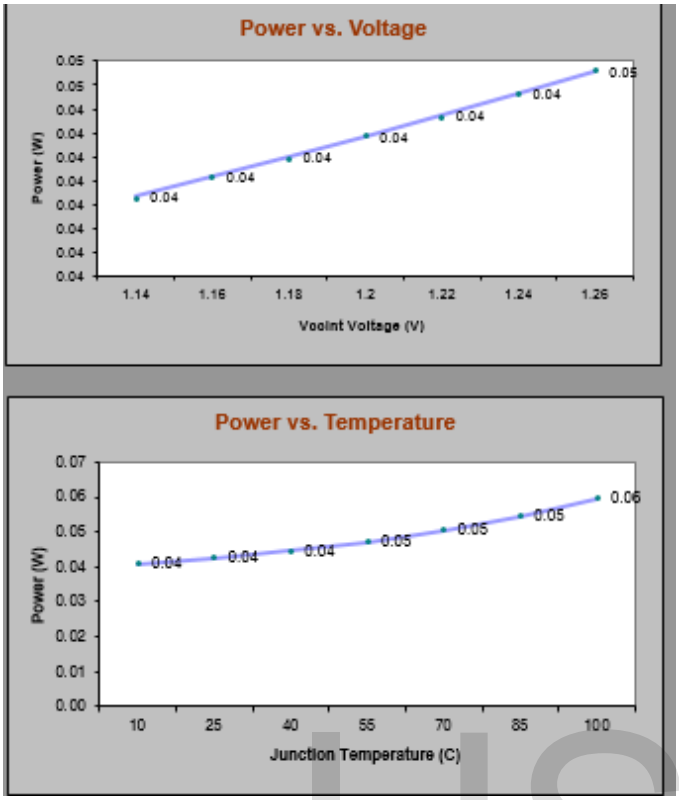

Fig.6 output of scattered look-ahead pipelined IIR filter

7 CONCLUSION

In this paper, clustered look-ahead and scattered look-ahead pipelining methodologies are analyzed. In clustered look-ahead pipelining, sample rate is increased by a factor of M and critical loop has M delay elements. Stability of the filter may be changed after pipelining. The complexity of the Scatter look ahead approach is high, In 3- stage pipelined filter multiplier is pipelined by 3 stages. In general M stage pipelined filter multiplier is pipelined by M stages.

REFERENCES

[1] Ravinder Kaur, Ashish Raman, "Design and Implementation of High Speed IIR and FIR Filter using Pipelining," International Journal of Computer Theory and Engineering, vol.3, No.2, April 2011.

[2] Chi-Jui Chou, Satish Mohanakrishnan, Joseph B.Evans,"FPGA Implementation of Digital Filters,", Proc.ICSPAT'93.

[3] Harish V.Dixit, Dr.Vikas Gupta,"IIR Filters using Xilinx System Generator for FPGA Implementation,"International Journal of Engineering Research and Applications, vol.2, Issue 5, September- October 2012, pp.303-307.

[4] Anatoli Sergyienko, Volodymir Lepekha, Juri Kanevski, Przemyslaw Soltan," Implementation of IIR Digital Filters in FPGA".

[5] Yen-Liang Chen, Chun-Yu Chen, Kai-Yuan Jheng, and An-Yeu(Andy)

[6] Wu, " A Universal Look-Ahead Algorithm for Pipelining IIR Filters," VLSI design, Automation and Test, 2008,IEEE International Symposium.

[7] K.K.Parhi and D.G.Messerschmitt," Pipeline Interleaving and Parallelism in Recursive Digital Filters- Part I: Pipelining using scattered look-ahead and decomposition," IEEE Trans.Acoustics, Speech, Signal Processing, vol.37,pp.1099-1117, July 1989.

[8] K.K.Parhi, VLSI Digital Signal Processing System Design and Implementation, John Wiley & Son, Inc., New York,1999.

[9] Michal D. Ciletti, Advanced Digital Design with the VERILOG HDL, Prentice-Hall of India Private Limited, NewDelhi, 2005.

[10] Michal Francis,"Infinite Impulse Response Filter Structures in Xilinx FPGAs", White Paper 330(v1.2) August 10, 2009